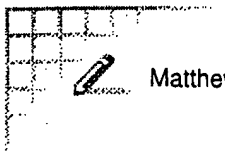


Matthew C Nicholls
01:03 PM

To: /Burlington/IBM@IBMUS
cc:
From: Matthew C Nicholls/Burlington/IBM@IBMUS
Subject: Multipass etch / implant write up

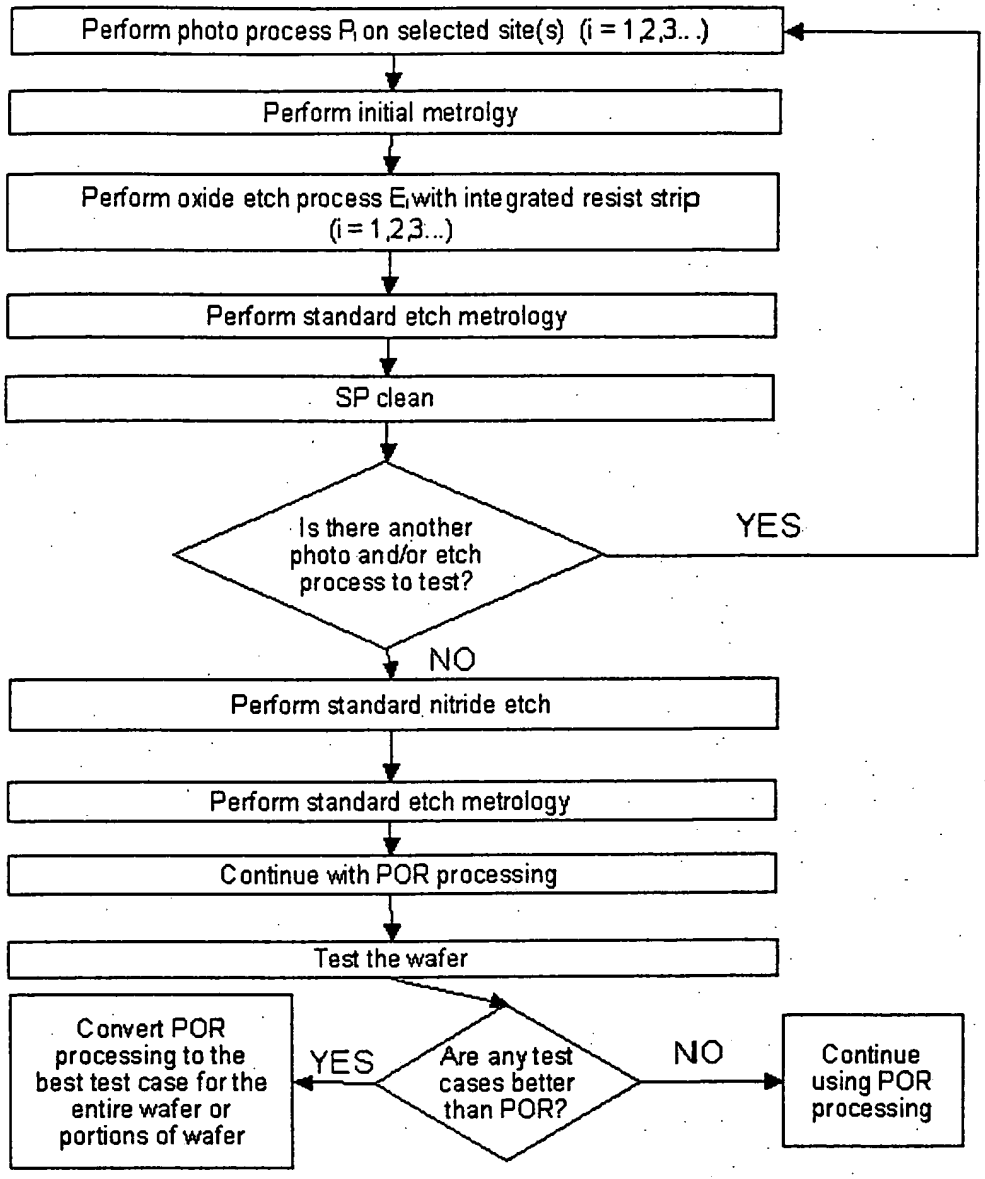
Here is an updated version of the write up with more pictures, flowsheets, and precise wording. I will submit the claims and the differences later this afternoon.

1. Describe your invention, stating the problem solved (if appropriate), and indicating the advantages of using the invention.

Patterning silicon wafers takes 2 coordinated steps, photolithography, which prints the desired image into photoresist (a photoactive and etch resistant material), and etch, which tranfers the initial image into the substrate (normally oxide or silicon). Lithography is a selective process that can be controlled field by field; etch, however, affects the entire wafer. This invention allows the user to manipulate several different etch processes (etch variables can include tooltype, temperature, time, chemical feed, etc) on a single wafer.

The resist is selectively exposed during the lithography step resulting in a combination of patterned and unpatterned portions on the wafer. When this wafer is etched or implanted only the exposed regions will be affected. The resist can be stripped from the wafer and the selective exposure can be repeated (leaving the previous fields or chips unexposed or covered in resist). The newly exposed fields can then be subject to a varied etch process. This process can be repeated several times until the desired conditions are attained at which point the wafer is shipped out of etch for deposition.

Basic Flowsheet



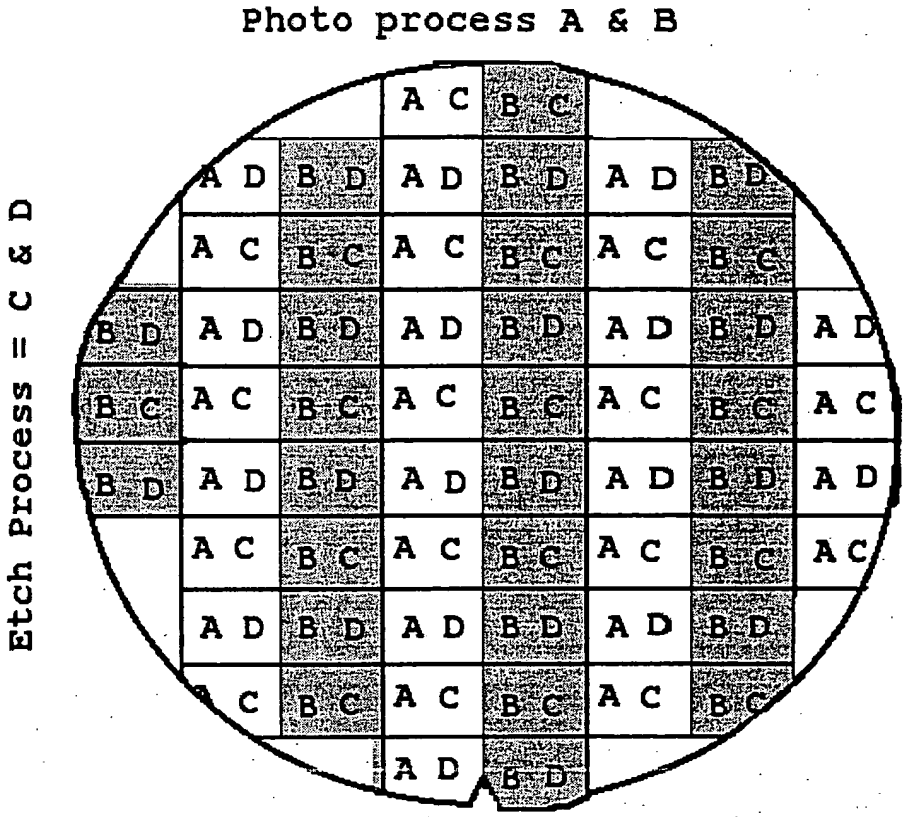

This invention will provide an improvement for many current manufacturing problems by allowing selective etch treatment. Common problems in a wafer line include:

*Etch Regionality Effects - features etch more rapidly in the center of the wafer resulting in unetched features on the outside of the wafer or overetched features in the center

Solution: multiple passes w/ slighly more aggressive etchs toward the outer portion of the wafer.

* Line Tailoring - Polysilicon gates, which are the main contributor to semiconductor speed, are carefully manipulated so that the critical dimension provides the optimum device speed. This is currently accomplished by striping wafers with different image sizes. There is a seperate feedback step from etch at which point the engineer decides the proper etch process based on photo and etch performance. An engineer could use this process to run wafers varying the lithography as well as the etch to determine the optimum process more quickly.

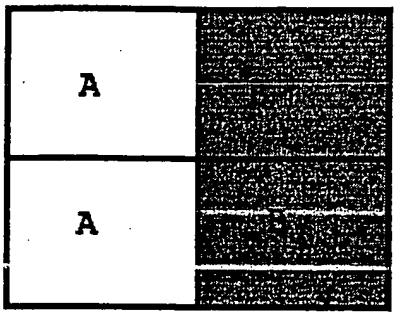
Wafer with 2 photo and 2 etch processes




* Multi--Part Number Wafers - Multiple part number wafers are wafers containing more than one customer design. This can mean multiple customer Rits produced on 1 reticle in order to determine the optimum design, or chips being manufactured for different customers combined on the same wafer (often used with very small chips). These rits can be different due to design variations which may require specific processes. For example, designers are free to utilize pattern densities varying by up to 300% at certain photo levels. Due to etch loading, nested/iso offsets and the like, processing two vastly different designs can push a process to its breaking point when trying to take both very dense and very sparse conditions into account. Currently process engineers cannot compensate for these differences; rather, they would be forced to use a process to optimize the yield on one of the designs, potential forfeiting the other design, negating the benefit of the multi-part number wafer. With this invention, process conditions uniquely suited to the requirements of the individual parts can be utilized, thus ensuring optimal processing.

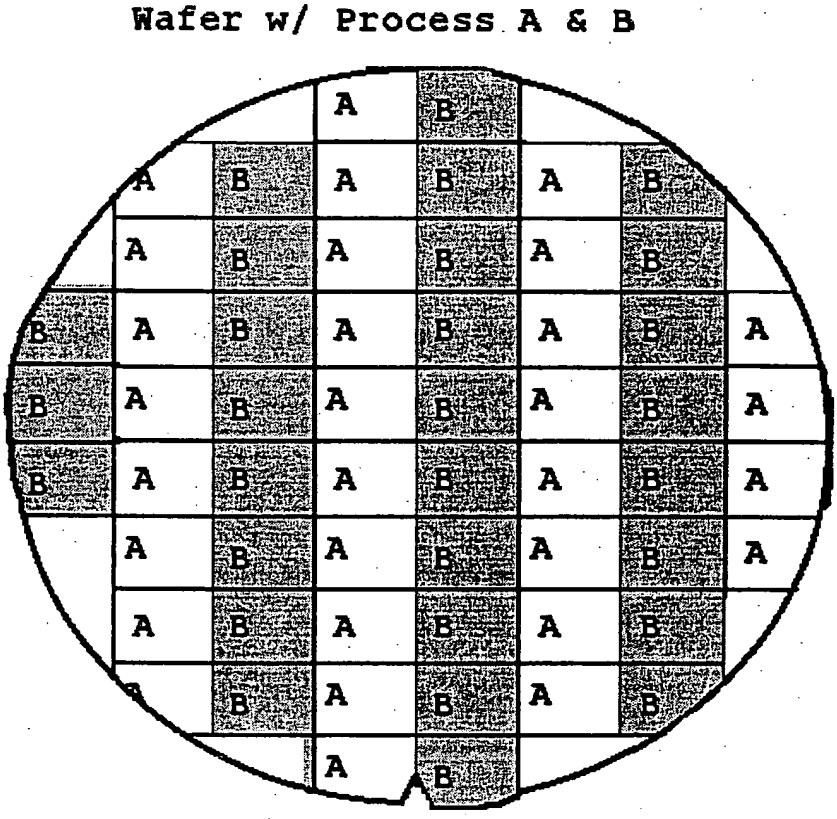
This invention will enable the manufacturer to alter processes for specific fields/chips to produce each part as desired. The process can be manipulated at the lithography, etch, or implant step enabling complex differences on a single reticle design. As wafer sizes increase and more part numbers are linked, it will become more and more difficult to group parts with similar pattern densities and designs, making this a more important option for improving yields and manufacturability.

Reticle with Design A and B

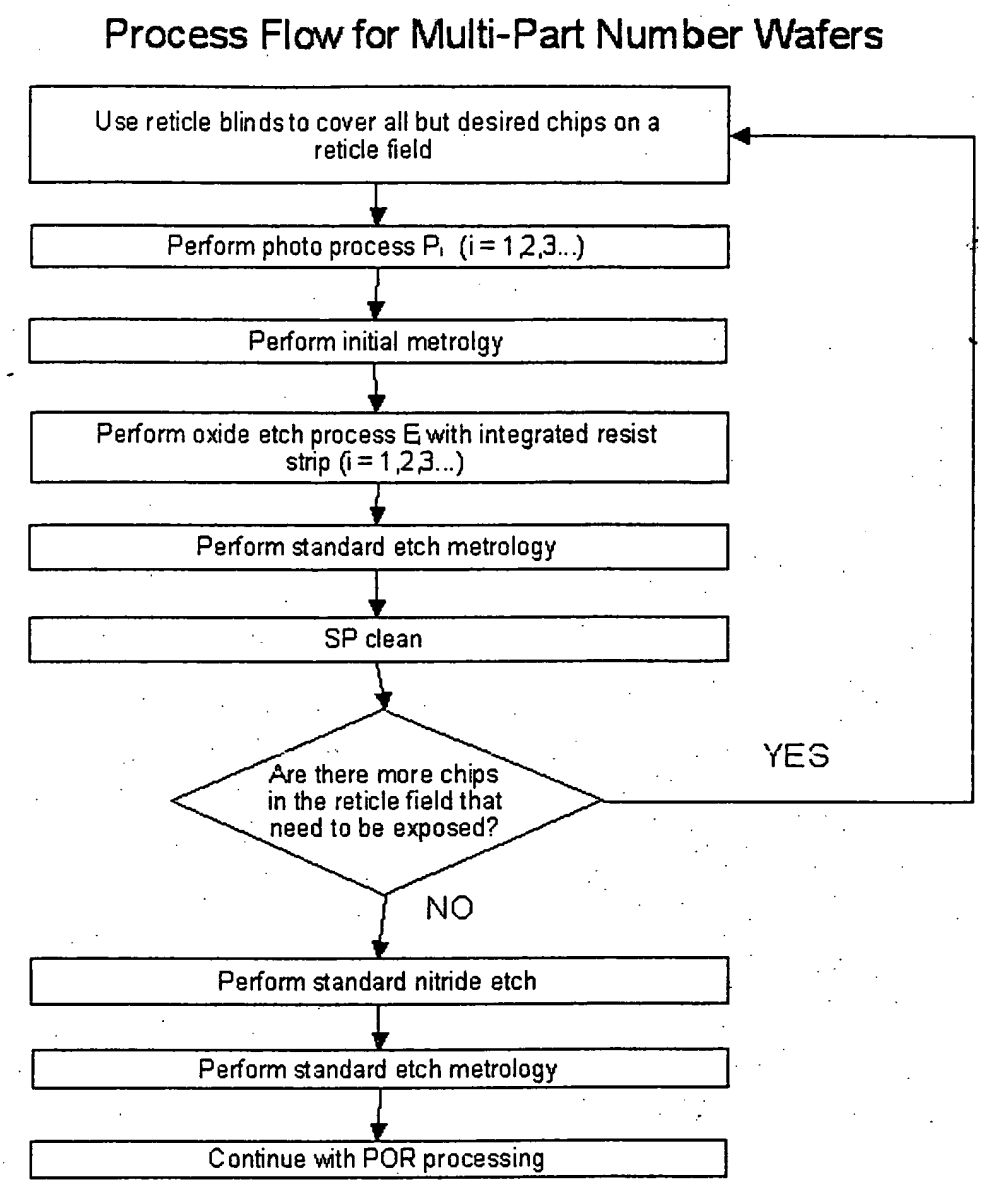



Wafer with Design A and B

Wafer with Design A and B




Flowsheet

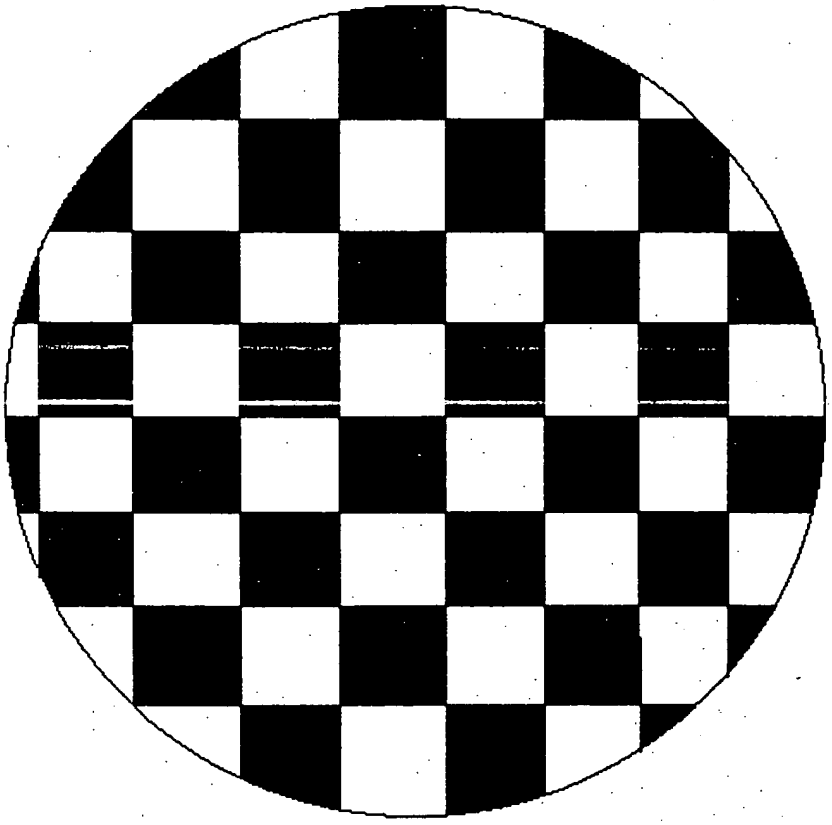



2. How does the invention solve the problem or achieve an advantage,(a description of "the invention", including figures inline as appropriate)?
The main advantage that this invention provides is the added flexibility for the etch engineer to experiment and use creative etch process to eliminate problems or to create new solutions on a wafer.

One problem solved is the large number of wafers routinely scrapped for etch experiments. Most etch experiments require many wafers to make a conclusion due to experimental variability and the reduction in raw materials will be increasingly valuable with the increase of wafer size. An experiment can consist of 2 wafers passing through photo and etch 5 times each instead of 10 wafers with one pass each. This advantage will be even more aparent with the advent of 300mm production due to the high cost of wafers.

Example of a possible photo pattern - the patterned white areas will be etched / transferred into the

substrate.



White - Exposed
Black - Blanket Resist

3. If the same advantage or problem has been identified by others (inside/outside IBM), how have those others solved it and does your solution differ and why is it better?
In order to determine the exact critical dimension for gates line tailoring (see above) is required. This is done by striping the wafer with different image sizes at photo. This experiment will allow engineers to vary etch as well to attain a more complete experiment while reducing the number of wafers which must be broken for cross-sectional analysis, as one wafer can contain many experimental cells.

Multi-part number wafers are being processed but currently there is no way to compensate for different etch requirements in different designs. With this experiment designs with slightly different processes can be included on the same wafer.

4. If the invention is implemented in a product or prototype, include technical details, purpose, disclosure details to others and the date of that implementation.
N/A

Matthew C. Nicholls
Process Engineer
e-mail: mcnichol@us.ibm.com